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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,065	12/09/2003	Aaron Christoph Sawdey	ROC920030094US1	3757

7590 03/16/2006

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EXAMINER	
BARTON, JONATHAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,065	SAWDEY, AARON CHRISTOPH	
	Examiner	Art Unit	
	Jonathan Barton	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5-7, 10-11, 15-17, 19-20, 22, 26-28, 30-31 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Witt (US 5,623,627).

a. As for claim 1 Witt discloses

i. at least one processor (Col 2 Lines 45-47);

ii. a memory (Col. 4 Lines 15-17);

iii. a first cache for temporarily holding portions of said memory, said first cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines (Col. 2 Lines 47-49); and

iv. a second cache for temporarily holding portions of said memory, said second cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines (Col. 2 Lines 54-58, 60-62);

v. wherein said associativity sets of said first cache and said associativity sets of said second cache correspond to a plurality of congruence groups, each congruence group containing a respective

plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache (Col. 5 Lines 60-67);

vi. wherein addresses corresponding to each respective associativity set of said first cache are allocated among the plurality of associativity sets in said second cache within the same congruence group as the respective associativity set of said first cache (Col. 6 Lines 19-25).

b. As for claim 11 Witt discloses

vii. at least one processor core (Col 2 Lines 45-47);

viii. first cache accessing logic for accessing a first cache, said first cache temporarily holding portions of a memory (Col. 2 Lines 47-49),

ix. said first cache accessing logic determining an associativity set of said first cache which corresponds to an input address generated by said processor core from among a plurality of associativity sets of said first cache, each associativity set containing one or more respective cache lines (Col. 2 Lines 47-49); and

x. second cache accessing logic for accessing a second cache, said second cache temporarily holding portions of said memory (Col. 2 Lines 54-58, 60-62),

xi. said second cache accessing logic determining an associativity set of said second cache which corresponds to said input address generated by said processor core from among a plurality of associativity sets of said

second cache, each associativity set containing one or more respective cache lines (Col. 2 Lines 54-58, 60-62);

xii. wherein said associativity sets of said first cache and said associativity sets of said second cache correspond to a plurality of congruence groups (Col. 5 Lines 60-67),

xiii. each congruence group containing a respective plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache (Col. 5 Lines 60-67);

xiv. wherein addresses corresponding to each respective associativity set of said first cache are allocated among the plurality of associativity sets in said second cache within the same congruence group as the respective associativity set of said first cache (Col. 6 Lines 19-25).

c. As for claim 22 Witt discloses

xv. responsive to an input address, determining an associativity set of a first cache which corresponds to said input address from among a plurality of associativity sets of said first cache, each associativity set containing one or more respective cache lines (Col. 2 Lines 47-49);

xvi. responsive to said step of determining an associativity set of a first cache, determining whether the associativity set determined by said step of determining an associativity set of a first cache contains data corresponding to said input address (Col. 2 Lines 47-49);

xvii. responsive to said input address, determining an associativity set of a second cache which corresponds to said input address from among a plurality of associativity sets of said second cache, each associativity set containing one or more respective cache lines (Col. 2 Lines 54-58, 60-62);

xviii. responsive to said step of determining an associativity set of a second cache, determining whether the associativity set determined by said step of determining an associativity set of a second cache contains data corresponding to said input address (Col. 2 Lines 54-58, 60-62);

xix. wherein said associativity sets of said first cache and said associativity sets of said second cache correspond to a plurality of congruence groups, each congruence group containing a respective plurality of associativity sets of said first cache and a respective plurality of associativity sets of said second cache (Col. 5 Lines 60-67);

xx. wherein addresses corresponding to each respective associativity set of said first cache are allocated among the plurality of associativity sets in said second cache within the same congruence group as the respective associativity set of said first cache (Col. 6 Lines 19-25).

d. As for claim 31 Witt discloses

xxi. at least one processor (Col 2 Lines 45-47);

xxii. a memory (Col. 4 Lines 15-17);

xxiii. a first cache for temporarily holding portions of said memory, said first cache containing a plurality of addressable associativity sets, each

associativity set containing one or more respective cache lines (Col. 2 Lines 47-49); and

xxiv. a second cache for temporarily holding portions of said memory, said second cache containing a plurality of addressable associativity sets, each associativity set containing one or more respective cache lines (Col. 2 Lines 54-58, 60-62);

xxv. wherein each said associativity set of said first cache corresponds to a respective plurality of addresses of data storable in the associativity set of said first cache (Col. 2 Lines 47-49), and

xxvi. each said associativity set of said second cache corresponds to a respective plurality of addresses of data storable in the associativity set of said second cache (Col. 2 Lines 54-58, 60-62);

xxvii. wherein addresses corresponding to each respective associativity set of said first cache are allocated among a respective plurality of associativity sets in said second cache (Col. 6 Lines 19-25);

xxviii. wherein addresses corresponding to each respective associativity set of said second cache are allocated among a respective plurality of associativity sets in said first cache (Col. 6 Lines 19-25).

e. As for claims 5, 15, 26 and 34 Witt discloses

xxix. data is not duplicated in said first and second caches (Col. 6 Lines 39-40).

f. As for claims 6, 16, 27 and 35 Witt discloses

xxx. said first cache is at a higher level than said second cache (Col. 2 Lines 48-58).

g. As for claims 7, 17, 28 and 36 Witt discloses

xxxi. said second cache is a victim cache of said first cache (Col. 6 Lines 40-44).

h. As for claims 9 and 29 Witt discloses

xxxii. said first and second caches are addressable using real memory addresses (Col. 4 Lines 15-24).

i. As for claims 10, 19 and 30 Witt discloses

xxxiii. each said associativity set in said first cache contains a respective plurality of cache lines, and each said associativity set in said second cache contains a respective plurality of cache lines (Col. 6 Lines 29-32).

j. As for claim 20 Witt discloses

xxxiv. said chip includes at least one of said first cache and said second cache (Col. 5 Lines38-43).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 8-9, 12-14, 21, 23-25, 29 and 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt (US 5,623,627) in view of Lane (US 2004/0225859)

k. As for claims 2, 12, 23 and 32 Witt fails to disclose the following limitation, which is taught by Lane:

xxxv. addresses corresponding to each respective associativity set of said first cache are allocated among the plurality of associativity sets in the second cache within the same congruence group using a hashing function of at least some address bits other than address bits used to determine the respective associativity set (Lane Par. 31 and 32).

xxxvi. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the hashing function taught by Lane with the cache system disclosed by Witt because both systems are cache organization systems and using the hashing function provides a simple and convenient method of addressing between the memory units.

l. As for claims 3, 12, 24, and 33 Lane teaches

xxxvii. said hashing function is a modulo-N function, where N is the number of associativity sets of said second cache in said congruence group (Par. 31, 32).

m. As for claims 4, 14 and 25 Lane teaches

xxxviii. each said congruence group contains M associativity sets of said first cache and N associativity sets of said second cache, wherein the greatest common factor of M and N is one (Par. 33, 36).

n. As for claim 8 Lane teaches

xxxix. said digital data processing device comprises a third cache, said third cache being at a level higher than said first cache and said second cache (Par. 29).

o. As for claim 21 Lane teaches

xl. said chip includes a plurality of processor cores, said plurality of processor cores sharing said first and second caches (Par. 29).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Barton whose telephone number is 571-272-8157. The examiner can normally be reached on Monday - Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Barton
Examiner
Art Unit 2186

JB

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100